REMARKS/ARGUMENTS

Claims 18-30 are currently pending, and no amendment is made in this response. Applicants respectfully request reconsideration in light of the following remarks.

Rejection of Claims 18-30

Claims 18-30 are rejected under 35 USC 102(a) as being anticipated by Sun et al. (USPN 6,401,221; hereinafter "Sun") under a new ground of rejection. Applicants respectfully traverse the rejection for the following reasons.

I. No "Configurable Logic Array"

In the Office Action (paragraph 3, page 2), the Examiner equates Applicants' claimed "configurable logic array" with the (programmable) flash memory in the cited Sun prior-art document. Applicants disagree. Applicants respectfully note that the mentioned equating by the Office Action is contrary to the knowledge of those skilled in the electronics field, now, and at the time of the invention.

The claimed "configurable logic array" is known in the electronics field, also, as a programmable logic device (PLD), field programmable gate array (FPGA) or programmable logic array (PLA) (see paragraph [0003] of the specification). A person having skill in the pertinent art recognizes that a "configurable logic array" is dramatically and fundamentally distinct from a (programmable) flash memory (or other volatile/non-volatile memory), at least, from the following two viewpoints.

First of all, with respect to the architecture, a "configurable logic array" is a device having a structure different from that of a flash memory (or other memory device). The configurable logic array generally consists of two main components: a logic plane and output logic macrocells (see, for example, Exhibit A). Specifically, the logic plane is a memory array that routs signals present on the devices' pins to the output logic macrocells. On the other hand, a flash memory (or other memory device) has a simple structure that merely consists of an array of memory cells.

Second, with respect to function or usage, the "configurable logic array" has a usage which can be considered more powerful than that of a (programmable) flash memory (or other memory device). A configurable logic array is primarily used to build a sequential logic, with an output that depends not only on the present input(s) but also on the history of the previous input(s). To the contrary, a (programmable) flash memory (or other memory device) may be used typically just for storing data.

As a consequence of the claimed "configurable logic array" being dramatically and fundamentally distinct from a (programmable) flash memory for the foregoing reasons, and of the cited Sun prior art not disclosing the claimed "configurable logic array" or the like, Applicants therefore respectfully submit that the claimed invention is not anticipated by the cited prior-art content of Sun.

II. No "Configuration Load Program" and No "Accessing" of a "Configuration Data"

Furthermore, in the Office Action (page 3), the Examiner equates the claimed accessing of a "configuration data" (of the configurable logic array) with the fetching of instructions from a memory in the cited prior-art disclosure of Sun. Applicants disagree with this equating based upon at least a rationale similar to that discussed above; that is, the "configurable logic array" in the claimed invention is dramatically and fundamentally distinct from a (programmable) flash memory as in the cited prior art, according to one or more of an architectural viewpoint and a functional/usage viewpoint.

Moreover, Applicants respectfully disagree with the asserted equating between the claimed "configuration data" and the "instructions" of Sun. It is well known in the art that "instructions" are more or less directly utilized to cause a processor (e.g., CPU) to perform specific operations. Quite to the contrary, "configuration data" contains and conveys information that is passively operable by a processor (e.g., CPU) or control logic.

Applicants respectfully note that it is illogical or even chaotic to replace Sun's "instructions" with the claimed "configuration data." Following such a replacement, to the extent even hypothetically sensical, the Sun system would cease to function as a consequence of the "configuration data" not causing the processor (e.g., CPU) to perform any operation.

As the "configuration data" term of Applicants' claims is quite distinct from the "instructions" term of Sun in one or more of essence

and substance, it may be concluded without doubt that the claimed "configuration data" in a configurable logic array cannot be likened or equated to "instructions" in the flash memory of Sun.

Further, as for the presently presented "configuration load program" term in the independent claims, using the same rationale as set forth above, it may be comfortably concluded without hesitation that the disclosure of Sun also does not anticipate the claimed "configuration [data] load program" simply because, for example, the cited prior art of Sun does not disclose any configurable logic array.

Thus, independent Claims 18 and 26 are not anticipated by the cited prior art of Sun. Moreover, the respective dependent claims are also patentable over the cited prior art on the same rationale discussed above, and further by operation of the totality of features recited in each of them. For the foregoing reasons, accordingly, it is respectfully submitted that the current invention specified by Claims 18-30 is patentable over the cited prior art.

Conclusion

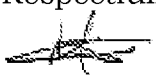
In light of the above remarks, Applicants respectfully submit that Claims 18-30 as currently presented are in condition for allowance. Accordingly, reconsideration is respectfully requested.

Should the Examiner believe that a telephone conference with Applicants' representative would be helpful to advance the prosecution of the application, or for any other reason, he or she is

kindly invited to contact the undersigned with any such concerns or questions.

The Commissioner is hereby authorized to charge any needed fees to deposit account 50-1600.

Respectfully submitted,



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